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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,420	04/13/2004	Seung-hwan Lee	SAM-0554	4026

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/823,420	LEE ET AL.
	Examiner	Art Unit
	Andy Huynh	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *26-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated 07/29/2005, Applicant has elected Invention of Group I (Claims **1-25**) drawn to a device without traverse is acknowledged. Accordingly, claims **26-37** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **26-37**, drawn to a method.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREAN, 03-30614 on 05/14/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 11/12/2004. The references cited on the PTOL 1449 form have been considered.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 4, 8, 9, 12, 24 and 25** are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et al. (USP 6,187,642 hereinafter referred to as "Yu").

Regarding claim **1**, Yu discloses in Figs. 2-6 and the corresponding texts as set forth in col. 2, line 50-col. 3, line 49, a method of fabricating a metal-oxide semiconductor (MOS) transistor having an elevated source/drain structure, comprises:

forming a gate dielectric/oxide 34 on an active region of a semiconductor substrate 32 and forming a gate electrode 35 on the gate dielectric/oxide;

forming a first gate spacer 48 on lateral side surfaces of the gate electrode;

forming a first epi-layer 52 on the semiconductor substrate;

forming a second gate spacer 55 on lateral side surfaces of the first gate spacer; and

forming a second epi-layer 58 on the first epi-layer.

Regarding claim **4**, Yu discloses in Figs. 2-6 the method further comprises: ion-implanting a dopant 53 in the semiconductor substrate to form a source/drain extension layer 54

after the first epi-layer is formed; and ion-implanting a dopant 60 in the semiconductor substrate to form a deep source/drain layer 54 after the second epi-layer is formed.

Regarding claims **8-9 and 12**, Yu discloses at least one of the first epi-layer and second epi-layer comprises silicon (col. 3, lines 6-9); at least one of the first epi-layer and second epi-layer is grown in accordance with a chemical vapor deposition process (col. 3, line 16).

Regarding claims **24 and 25**, Yu discloses in Figs. 2-6 the method further comprises forming a source/drain layer by in-situ doping a dopant in at least one of the first epi-layer and second epi-layer during forming the first epi-layer or second epi-layer; forming a source/drain layer by ion-implanting a dopant in at least one of the first epi-layer or second epi-layer during forming the first epi-layer or second epi-layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (USP 6,187,642 hereinafter referred to as "Yu") in view of Lin (USP 6,727,543).

Yu discloses the all claimed limitations except for the method further comprises: forming a first gate oxide on the lateral side surfaces of the gate electrode before the first gate spacer is formed; and forming a second gate oxide on the lateral side surfaces of the first gate spacer

before the second gate spacer is formed. Lin teaches in Figs. 2A-2D a method of fabricating a MOS transistor comprises forming a first gate oxide 230 on the lateral side surfaces of the gate electrode 210 before the first gate spacer 240 is formed; and forming a second gate oxide 250 on the lateral side surfaces of the first gate spacer before the second gate spacer 260 is formed. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to utilize the teaching of forming a MOS transistor comprising forming a first gate oxide on the lateral side surfaces of the gate electrode before the first gate spacer is formed; and forming a second gate oxide on the lateral side surfaces of the first gate spacer before the second gate spacer is formed, as taught by Lin to incorporate into Yu's method to arrive the claimed limitation in order to obtain a bigger spacer for the logic device because the requirement of the scale of the spacers is different for the memory device and for the periphery device (col. 1, lines 16-36).

Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (USP 6,187,642 hereinafter referred to as "Yu") in view of Chau et al. (USP 6,326,664 hereinafter referred to as "Chau").

Yu discloses the all claimed limitations except for the method further comprises: forming a first poly-layer on the gate electrode while the first epi-layer is formed; and forming a second poly-layer on the first poly-layer while the second epi-layer is formed. Chau teaches in Figs. 3B-3F a method of fabricating a transistor 40 comprises forming semiconductor material 314 on the gate electrode 306 while depositing into recesses 312, and forming silicide 320 on the

semiconductor material of the gate electrode while depositing onto deposited semiconductor material on source/drain contact region to significantly reduce the device contact resistance (col. 4, line 37-col. 7, line 25). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to utilize the teaching of a method of fabricating a transistor 40 comprises forming semiconductor material on the gate electrode while depositing into recesses, and forming silicide on the semiconductor material of the gate electrode while depositing onto deposited semiconductor material on source/drain contact region, as taught by Chau to incorporate into Yu's method to arrive the claimed limitation in order to significantly reduce the device contact resistance.

Claims **5-7, 10, 11 and 13-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (USP 6,187,642 hereinafter referred to as "Yu").

Regarding claims **5-7, 11, 14, 19 and 22**, Yu discloses the all claimed limitations except for a thickness of the first epi-layer is about 20 to 30 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer; a thickness of the second epi-layer is about 70 to 80 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer; wherein the second gate spacer is four to six times wider than the first gate spacer; the low pressure chemical vapor deposition process is conducted under 10 to 30 torr; the ultra-high vacuum chemical vapor deposition process is conducted under 1 0^{-4} to 10^{-5} torr. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a thickness of the first epi-layer is about 20 to 30

% of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer; a thickness of the second epi-layer is about 70 to 80 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer; wherein the second gate spacer is four to six times wider than the first gate spacer; the low pressure chemical vapor deposition process is conducted under 10 to 30 torr; the ultra-high vacuum chemical vapor deposition process is conducted under 1 0^{-4} to 10^{-5} torr, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims **10, 13, 16, 18 and 21**, Yu discloses the all claimed limitations except for at least one of the first epi-layer and second epi-layer is formed using a source gas including dichlorosilane and HCI; or a source gas, including Si_2H_6; at least one of the first epi-layer and second epi-layer comprises silicon-germanium; at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCI, and GeH_4. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use at least one of the first epi-layer and second epi-layer is formed using a source gas including dichlorosilane and HCI; at least one of the tirst epi-layer and second epi-layer comprises silicon-germanium; at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCI, and GeH_4, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims **15 and 23**, Yu discloses the method further comprises: baking the semiconductor substrate or the first epi-layer at 800 to 900°C except for under a hydrogen

atmosphere for one to five minutes before the at least one of the first epi-layer and second epi-layer is formed. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to bake the semiconductor substrate or the first epi-layer under a hydrogen atmosphere for one to five minutes before the at least one of the first epi-layer and second epi-layer is formed, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Regarding claims **17 and 20**, Yu discloses at least one of the first epi-layer and second epi-layer is grown in accordance with a chemical vapor deposition process (col. 3, line 16).

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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08/05/05

Andy Huynh

Patent Examiner